REMARKS

Claims 1-4, 7-8, 11, 18-20, 23, 24, 33-36, 39-40, 43, 50-52, 55-56 and 65-66 were rejected under 35 U.S.C. 102(e) as being anticipated by Keashly et al., U.S. patent 6,330,289 B1. The remaining claims were rejected under 35 U.S.C. 103(a) as being unpatentable over Keashly et al. in view of Bae, U.S. patent 6,242,960 B1. Those rejections are respectfully traversed and reconsideration is requested.

Independent claims 1 and 33 are directed to a data transmitter which controls the transition time of a data signal, that is the time that it takes for the data signal to change from one state to the next. As illustrated in Figure 2, an input data signal din has very short transition times from low to high and from high to low. By contrast, the data signal dout has a substantially longer transition time t_r from low to high. This long transition time is obtained by applying the data signal to parallel delay circuits as illustrated, for example, in Figures 1 and 3. The data signal output from each of those delays has a transition time t_{r1} illustrated in Fig. 2. However, by summing the multiple delayed signals at a common output node, it can be seen that the combined transition time of the summed signals d1'-d4' provides the longer transition t_r of signal dout.

Neither of the cited references allows the determination of a transition time of a data signal.

The Keashly et al. invention is directed to a reduction of peak to average signal power where multiple correlated signals, such as those clocked by a common clock, are combined on a common channel. Keashly realized that the largest component of peak signal power occurs whenever a modulation symbol, which represents one or more data bits, goes through transition. The peak power problem is exacerbated when multiple signals have symbol transitions at the same time. See the left side of Figs. 2 and 3. Keashly concluded that the overall peak power could be reduced by spreading the peaks of the individual signals over time by staggering the transitions of the several signals. Note, however, that Keashly does not address the transition time of an individual signal, that is, the time that it takes for a data signal to change from one

state to the next, such as from low to high. In fact, each of the data inputs in Fig. 2 is illustrated to have a respective transition time at 112, 122 and 132 of zero. Whereas the present invention is directed to extending the transition time of a single data input, Keashly is directed to staggering transitions of multiple data inputs without regard to the transition times of the inputs.

Each of claims 1 and 33 recites that different delays are applied to a singular data input and that the delayed data signals are combined in a data output having a transition time determined by differences in delays applied to the data input. Keashly does not apply multiple delays to the same data input. Instead, Keashly applies different delays to different data inputs. Further, Keashly does not determine the transition time of the data output, that is, a rise time or fall time (page 1, line 7 of the present application) of the data output.

With respect to claims 18 and 50, prior art transition control systems control the transition time to be a fixed value, regardless of the bit time of the system. With a fixed transition time, a signaling system operating at a lower speed is forced to use a transition time optimized for the highest possible speed of operation, unduly stressing the bandwidth of the transmission medium. In accordance with claims 18 and 50, the transition time of the controlled data signal is proportional to bit time of the bit clock. As already discussed, Keashly does not address transition time of a data signal at all, so there can be no suggestion of transition time proportional to bit time.

Nor does Keashly teach the dependent claims. In particular, with respect to claims 2 and 34, Keashly includes no "common delay element" in series with each of the parallel delay elements.

With respect to claims 3, 19, 35 and 51, Keashly delays multiple clock signals and applies those delayed clocks to sample multiple, different data signals. In contrast, the present claims require that a single clock signal be delayed by parallel delay elements, those delayed versions of the single clock signal being used to sample a single data signal.

With respect to claims 4, 20, 36 and 52, the system of Keashly does not include plural driver circuits. Multiple bit streams are combined via combiner 60, and the combined signal is input to an amplifier 70.

With respect to claims 7, 23, 39 and 55, the claimed data signal is applied to all of the delay elements, while the system of Keashly applies different data signals to different delay elements as described above.

Claims 11 and 43 are further allowable for the same reasons 18 and 50 are allowable. In particular, there is no suggestion in Keashly of a transition time which is proportional to bit time.

There is no suggestion to combine Bae with Keashly, and even if combined, Bae fails to teach the deficiencies of Keashly discussed above.

The examiner cites Bae to cover a number of dependent claims that include CMOS inverters (claim 5), load capacitance (claim 6), a delay circuit to control supply voltage (claims 13 and 14), delay controlled by supply voltage (claim 12). Bae does disclose CMOS inverters. Bae, does not, however disclose the other elements. The passage cited by the examiner for capacitive load that controls delay describes load devices that provide current to differential amplifier 110, not capacitive loads that provide delay. The power supplies in the Bae reference, Vdd, Vcc, Vss, and Vref are all constant. There is no use of power supplies to vary delay in Bae. However, using both load capacitance and supply voltage to control delay is known in the prior art.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 12/30/3